



# LC7265

## Received Frequency Display for Radio Receivers

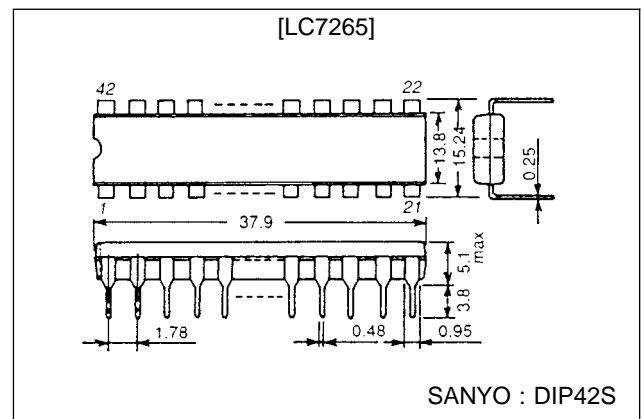
### Features

- Displays received frequency of each band of FM, MW, LW (LED static display).
- Counts local oscillation frequency and displays received frequency.
- Number of display digits : FM-5 digits, MW-4 digits, LW-3 digits.
- Covers intermediate frequencies shown below.
  - FM : +10.700, +10.725, +10.750, +10.675 MHz  
-10.700, -10.725, -10.675, -10.650 MHz
  - MW, LW : +450 kHz : 10 kHz step display  
+450 kHz : 1 kHz step display  
+455 kHz : 1 kHz step display  
+469 kHz : 1 kHz step display
- Contains blanking circuit to turn off display.
- Contains hold circuit to hold display contents.
- Uses crystal resonator having 7.2 MHz reference frequency.
- Uses LB3500 (+8 prescaler) jointly at the time of FM reception.
- Supply voltage  $V_{DD}$  : 4.5 V to 10 V

### Package Dimensions

unit : mm

#### 3025B-DIP42S



### Specifications

#### Absolute Maximum Ratings at $T_a = 25^\circ\text{C}$ , $V_{SS} = 0\text{ V}$

Parameter	Symbol	Conditions	Ratings	Unit
Maximum supply voltage	$V_{DD\text{ max}}$		-0.3 to +11	V
Input voltage	$V_{IN}$	All input pins	-0.3 to $V_{DD}+0.3$	V
Output voltage	$V_{O1}$	$X_{OUT}$ , $\overline{HLD}$ , 50 Hz, output: off	-0.3 to $V_{DD}+0.3$	V
	$V_{O2}$	Output pins other than $V_{O1}$	0 to 15	V
Allowable power dissipation	$P_d\text{ max}$	$T_a \leq 65^\circ\text{C}$	550	mW
Allowable power dissipation of segment outputs	$P_d\text{ (seg)1}$	MHz, $\overline{b\&c}$ , $\overline{b\&e}$ , $V_{DD} = 4.5$ to $6.5\text{ V}$ , $I_{OL} = 33\text{ mA}$	30	mW
	$P_d\text{ (seg) 2}$	Other outputs, $V_{DD} = 4.5$ to $6.5\text{ V}$ , $I_{OL} = 16.5\text{ mA}$	15	mW
	$P_d\text{ (seg) 3}$	MHz, $\overline{b\&c}$ , $\overline{b\&e}$ , $V_{DD} = 6.0$ to $10\text{ V}$ , $I_{OL} = 36\text{ mA}$	25	mW
	$P_d\text{ (seg) 4}$	Other outputs, $V_{DD} = 6.0$ to $10\text{ V}$ , $I_{OL} = 18\text{ mA}$	12	mW
Operating temperature	$T_{opr}$		-30 to +65	$^\circ\text{C}$
Storage temperature	$T_{stg}$		-40 to +125	$^\circ\text{C}$

## LC7265

### Allowable Operating Ranges at Ta = 25 °C, V<sub>DD</sub> = 4.5 to 10 V, V<sub>SS</sub> = 0 V

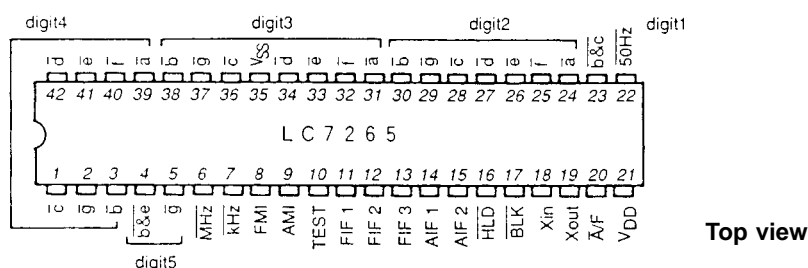
Parameter	Symbol	Conditions	min	typ	max	Unit
Supply voltage	V <sub>DD</sub>		4.5		10	V
Input high-level voltage	V <sub>IH1</sub>	$\bar{A}/F, \overline{BLK}$	0.7V <sub>DD</sub>		V <sub>DD</sub>	V
	V <sub>IH2</sub>	FIF1, FIF2, FIF3, AIF1, AIF2	0.9V <sub>DD</sub>		V <sub>DD</sub>	V
Input low-level voltage	V <sub>IL1</sub>	$\bar{A}/F, \overline{BLK}$	0		0.3V <sub>DD</sub>	V
	V <sub>IL2</sub>	FIF1, FIF2, FIF3, AIF1, AIF2	0		0.1V <sub>DD</sub>	V
Input frequency	f <sub>IN1</sub>	FMI, sine wave, capacitive coupling, V <sub>IN1</sub> = 0.7V <sub>p-p</sub>	1		18	MHz
	f <sub>IN2</sub>	AMI, sine wave, capacitive coupling, V <sub>IN2</sub> = 0.5V <sub>p-p</sub> *	0.5		3	MHz
	f <sub>IN3</sub>	X <sub>IN</sub>	0.2		7.5	MHz
Input amplitude	V <sub>IN1</sub>	FMI, sine wave, capacitive coupling, f <sub>IN1</sub> = 1 to 18 MHz	0.7		0.9V <sub>DD</sub>	V <sub>p-p</sub>
	V <sub>IN2</sub>	AMI, sine wave, capacitive coupling, f <sub>IN2</sub> = 0.5 to 3 MHz	0.5*		0.9V <sub>DD</sub>	V <sub>p-p</sub>
	V <sub>IN3</sub>	X <sub>IN</sub> , sine wave, capacitive coupling, f <sub>IN3</sub> = 0.2 to 7.5 MHz	1.0		0.9V <sub>DD</sub>	V <sub>p-p</sub>
Segment current	I <sub>seg1</sub>	MHz, b&e, b&c	0		30	mA
	I <sub>seg2</sub>	Other outputs	0		15	mA

\*: For f<sub>IN2</sub> = 0.5 MHz to 0.9 MHz and V<sub>DD</sub> = 8 to 10 V, V<sub>IN2</sub> min = 1.0 V<sub>p-p</sub> applies.

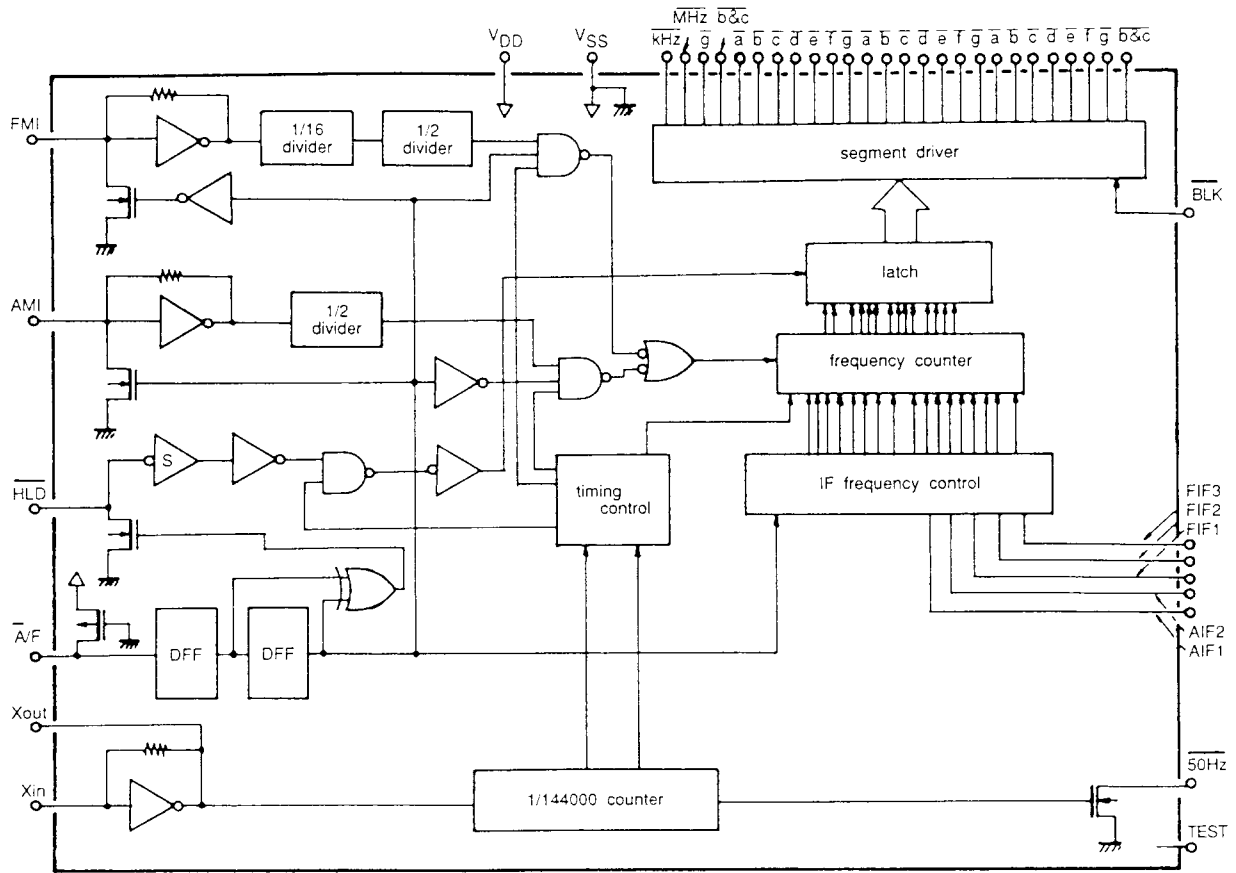
### Electrical Characteristics at Ta = 25 °C, V<sub>DD</sub> = 4.5 to 10 V, V<sub>SS</sub> = 0 V

Parameter	Symbol	Conditions	min	typ	max	Unit
Input high-level current	I <sub>IH1</sub>	FIF1, FIF2, FIF3, AIF1, AIF2 V <sub>I</sub> = V <sub>DD</sub>	0		10	μA
	I <sub>IH2</sub>	$\overline{BLK}$ V <sub>I</sub> = V <sub>DD</sub>	0		2	μA
Input low-level current	I <sub>IL1</sub>	FIF1, FIF2, FIF3, AIF1, AIF2 V <sub>I</sub> = V <sub>SS</sub>	0		10	μA
	I <sub>IL2</sub>	$\overline{BLK}$ V <sub>I</sub> = V <sub>SS</sub>	0		2	μA
	I <sub>IL3</sub>	$\bar{A}/F$ V <sub>I</sub> = V <sub>SS</sub>	20		500	μA
Input floating voltage	V <sub>IF</sub>	$\bar{A}/F$ V <sub>I</sub> = open	0.8V <sub>DD</sub>		V <sub>DD</sub>	V
Input/output high-level leakage current	I <sub>OFF</sub>	$\overline{HLD}$ , output off, V <sub>I</sub> = V <sub>DD</sub>	0		2	μA
Output low-level voltage	V <sub>OL1</sub>	$\overline{HLD}$ , output on, I <sub>O</sub> = 1 mA	0		1	V
	V <sub>OL2</sub>	b&e, b&c, MHz V <sub>DD</sub> = 4.5 to 10 V, I <sub>OL</sub> = 30 mA	0		0.7	V
	V <sub>OL3</sub>	Segments other than above V <sub>DD</sub> = 4.5 to 10 V, I <sub>OL</sub> = 15 mA	0		0.7	V
	V <sub>OL4</sub>	50 Hz, I <sub>O</sub> = 0.2 mA	0		1.0	V
Input high-level threshold voltage	V <sub>th</sub>	$\overline{HLD}$	0.4V <sub>DD</sub>	0.5V <sub>DD</sub>	0.7V <sub>DD</sub>	V
Output off leakage current	I <sub>OFF2</sub>	All segments output pins, V <sub>O</sub> = 13 V, output off	0		10	μA
Current drain	I <sub>DD</sub>	FM mode, $\bar{A}/F$ = open or V <sub>DD</sub> , f <sub>IN1</sub> = 18 MHz, 0.7V <sub>p-p</sub> or (AM mode, $\bar{A}/F$ = V <sub>SS</sub> , f <sub>IN2</sub> = 3 MHz, 0.5V <sub>p-p</sub> ) f <sub>IN3</sub> = 7.2 MHz, 1V <sub>p-p</sub> FIF1, FIF2, FIF3 = V <sub>DD</sub> AIF1, AIF2 = V <sub>DD</sub> $\overline{HLD}$ , $\overline{BLK}$ = V <sub>DD</sub> other pins open	0		18	mA

### Pin Assignment

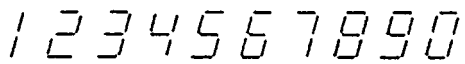


Equivalent Circuit Block Diagram



1. Display

1-1 Display font



1-2 Lighting system

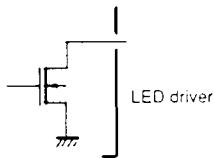
- Static lighting

1-3 Display range (High-order 1 digit : zero blanking)

- FM : 00.00 MHz to 199.95 MHz 50 kHz step
- MW, LW : 000 kHz to 1999 kHz 10 kHz or 1 kHz step

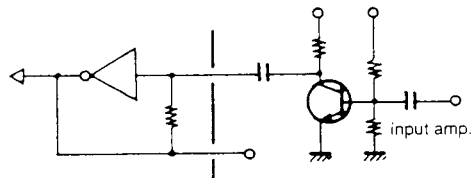
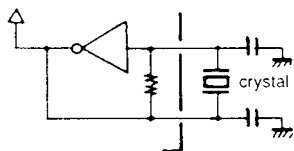
2. Pin Description

2-1 •  $\bar{a}$  to  $\bar{g}$ ,  $\bar{b\&c}$ ,  $\bar{b\&e}$ ,  $\overline{MHz}$ ,  $\overline{kHz}$  : LED



2-2 •  $V_{DD}$ ,  $V_{SS}$  : Power supply pins

2-3 •  $X_{IN}$ ,  $X_{OUT}$  : Crystal resonator or input amp pin



# LC7265

2-4 • FIF1, FIF2, FIF3 : FM IF select pins

FIF1	0	0	0	0	1	1	1	1
FIF2	0	0	1	1	0	0	1	1
FIF3	0	1	0	1	0	1	0	1
IF (MHz)	+10.700	+10.725	+10.675	+10.750	-10.700	-10.725	-10.675	-10.650

2-5 • AIF1, AIF2 : AM IF select pins

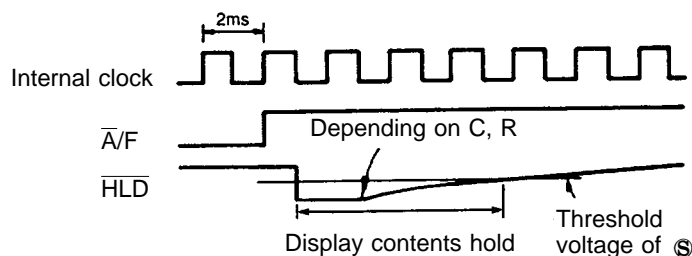
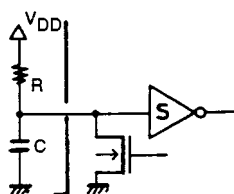
AIF1	0	0	1	1
AIF2	0	1	0	1
IF (kHz)	+450 (2)	+450 (1)	+455	+469

1 : High level ( $V_{DD}$ )  
0 : Low level ( $V_{SS}$ )

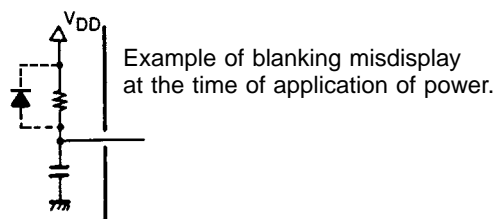
(Note) 450 kHz(1) : 10 kHz step display, others : 1 kHz step display

2-6 •  $\overline{HLD}$  : Display contents hold pin

Normally, this pin is set at high level. To hold display contents, this pin is set at low level. Connecting time constant circuit to this pin makes it possible to hold display contents for a certain period of time at the time of FM/MW, LW band selection.



2-7 •  $\overline{BLK}$  : Display blanking pin



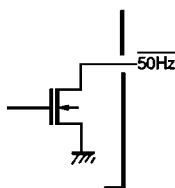
2-8 • FMI, AMI : Local oscillation signal input pins

FMI — For FM : 0.7Vp-p input sensitivity  
AMI — For MW, LW : 1.0Vp-p input sensitivity ( $V_{DD} = 8$  to 10 V,  $f_{IN} = 0.5$  to 0.9 MHz)  
0.5Vp-p input sensitivity (other than above)

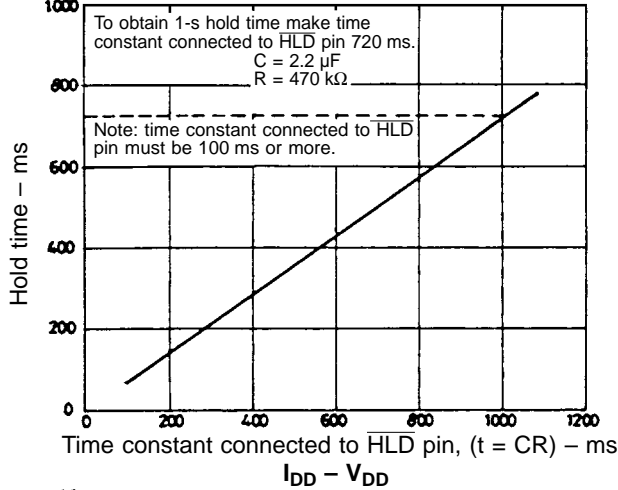
2-9 •  $\overline{A/F}$  : FM/MW, LW select pin

FM — Pin open or high level  
MW, LW — Low level

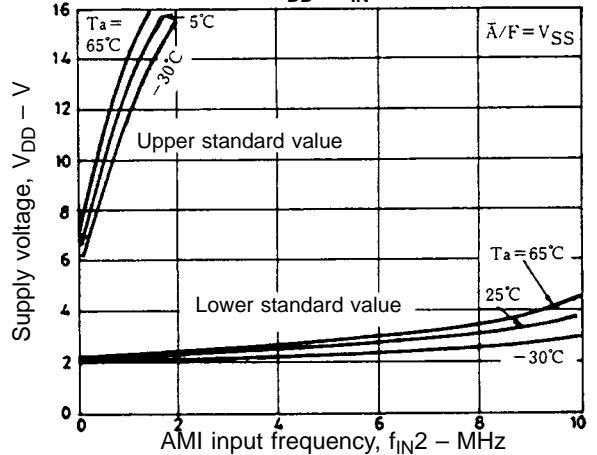
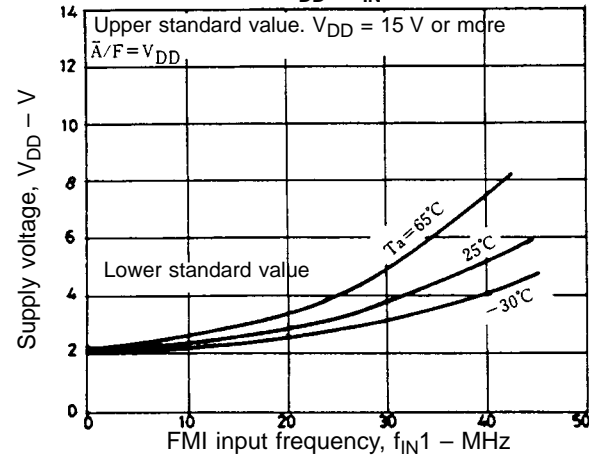
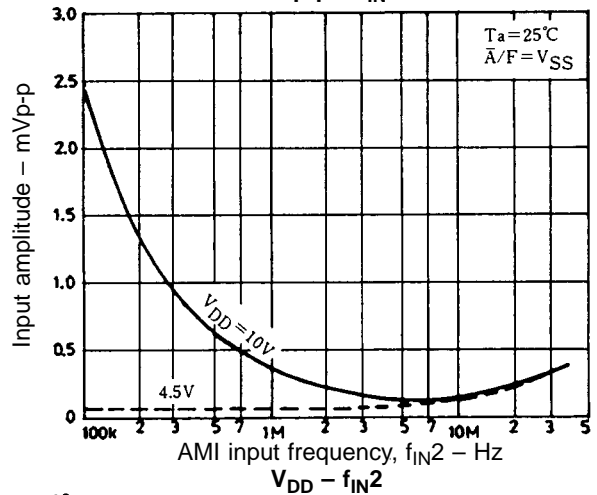
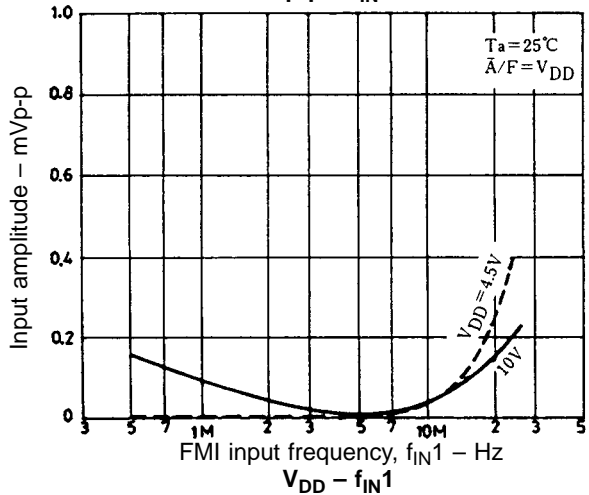
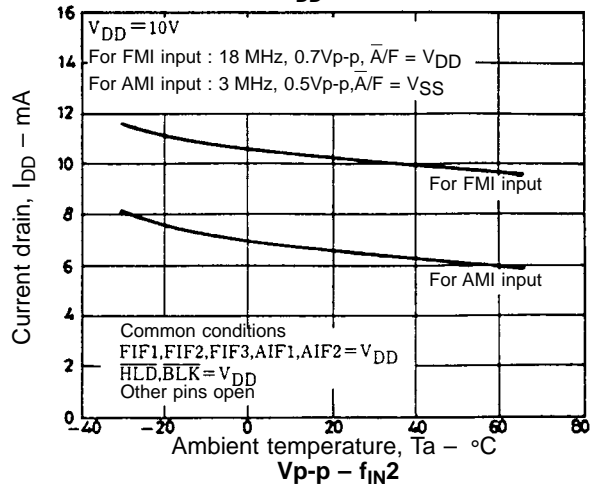
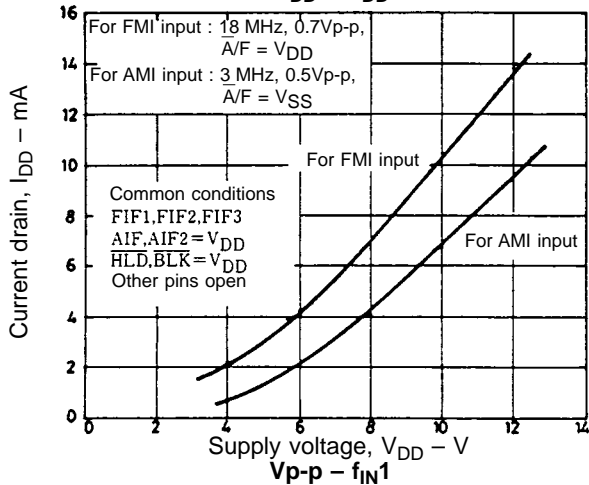
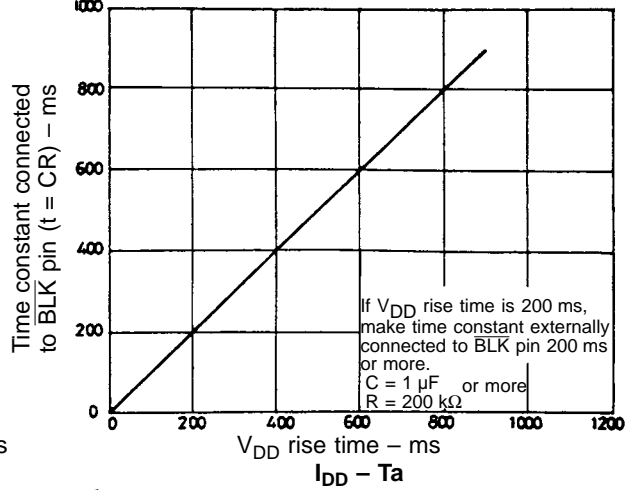
2-10 •  $\overline{50\text{Hz}}$  : 50 Hz time base output pin

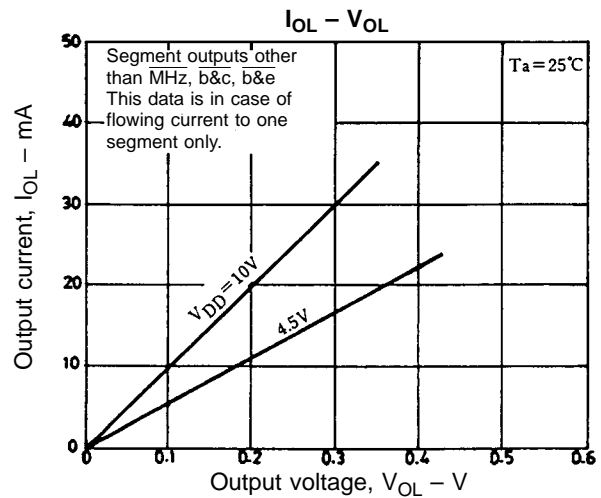
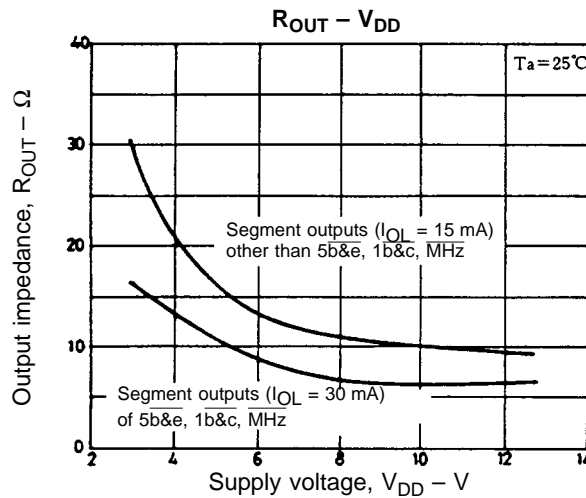
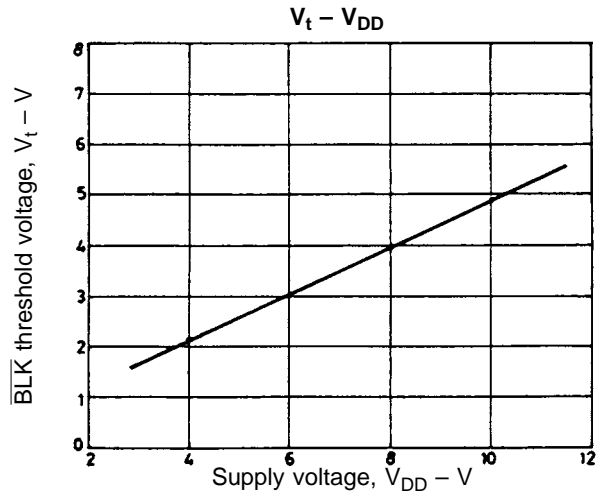
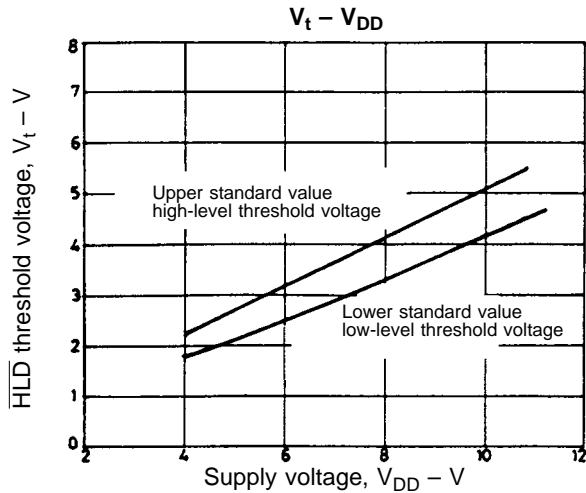


Hold time – time constant connected to  $\overline{\text{HLD}}$  pin



Time constant connected to  $\overline{\text{BLK}}$  pin –  $V_{DD}$  rise time





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